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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/646,193	BAIN, PETER	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44,46-50 and 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37 and 49* is/are allowed.

6)☒ Claim(s) *1-8,11-20,23-32,35,36,38-42,44-48 and 50-57* is/are rejected.

7)☒ Claim(s) *9,10,21,22,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amended application filed on 10/22/2007.

2. Claims 1-44, 46-50, and 57 are presented for examination.

   a. Currently, claims 45, and 51 are canceled.

   b. Claims 1, 13, 25, 33, 39-44, are amended.

   c. Previously, claims 37, and 49 have been allowed, and claims 9, 10, 21, 22, 33, and 34 have been objected.

Response to Arguments

3. Response to Objection to the Specification: Claim 39 has been amended to have "computer" readable medium instead of "machine" readable medium. The "computer" readable medium has antecedent basis in specification and therefore the objection is withdrawn.

4. Response to double Patenting rejection: The terminal disclaimer filed on 05/08/2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent No. 7, 107, 567 has been reviewed and is accepted. The terminal disclaimer has been recorded.

5. Response to 35 USC 101 rejection: Applicant's arguments have been fully considered but they are not persuasive.

Claims 25 and 39 recite "computer readable medium". Applicant's specification (page 12) noted as follows:

> Some embodiments of the present invention relate to computer readable media or computer program products that include program instructions and/or data (including data structures) for performing various computer-implemented operations. Examples of computer-readable media include, but are not limited to, magnetic media such as hard disks, floppy disks, and magnetic tape; optical media such as CD-ROM disks; magneto-optical media; semiconductor memory devices, and hardware devices that are specially configured to store and perform program instructions, such as read-only memory devices (ROM) and random access memory (RAM). The data and program instructions of this invention may also be embodied on a carrier wave or other transport medium (including electronic or optically conductive pathways).

According to the above portion of the specification, the "medium" covers "carrier wave", which is *not a **Manufacture** within the meaning of 101.* In such embodiment, the program is still unable to act as a computer component and have its functionality realized.

Applicants have not disavowed the non-statutory embodiment in specification. To overcome the rejection a clear *disavowal is needed*.

6. Response to 35 USC 112, second paragraph, rejection: Applicants have been amended the claims to overcome the rejection and therefore the rejection is withdrawn.

7. Response to 35 USC 103(a) rejection: Applicant's arguments have been fully considered but they are not persuasive.

d. Applicant's argued:

> Claim 1 requires an "electronic design suitable for direct compilation into a practical hardware implementation of the electronic design." The Office action at page 5 indicates that the electronic design could be a design for a hardware module or a software module, and that *Jakubowski* teaches a design for a software module. But, the specification makes clear that an "electronic design" generally refers to the logical structure of an electronic device such as an integrated circuit (page 9, line 33-page 10, line 9) that is implemented in hardware. "Electronic design" does not refer to a design for a software module, and thus any software module disclosed by *Jakubowski* cannot anticipate this element.

As admitted by applicants in their arguments:

> Generally, the obfuscation circuitry is automatically inserted in non-obfuscated versions of an electronic design (e.g., IP core) by the systems and methods of this invention, which are implemented as software programs (or combinations of hardware and software). Generally, an obfuscation system of this invention must first

In light of the specification, "electronic design" could also refer to a design for a software module (i.e. digital goods) of the reference.

e. Applicant's argued that the reference fails to teach ***adding obfuscation circuitry*** *to said electronic design to produce an obfuscated version of the electronic design.*

In response, the reference teaches:

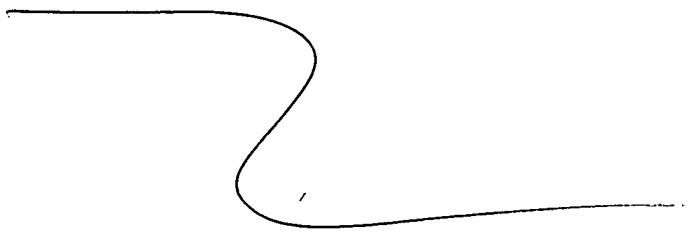
Col. 3 lines 64-66:

> 136(1)–136(N). Generally speaking, the obfuscator 134 automatically parses the original digital good 122 and applies selected protection tools 136(1)–136(N) to various portions of the parsed good in a random manner to produce

Col. 4 lines 5-9:

> The original digital good 122 represents the software product or data as originally produced, without any protection or code modifications. The protected digital good 124 is a unique version of the software product or data after the various protection schemes have been applied. The pro-

Further, the reference teaches "adding obfuscation circuitry" in digital goods using different tools as seen in the figure below:



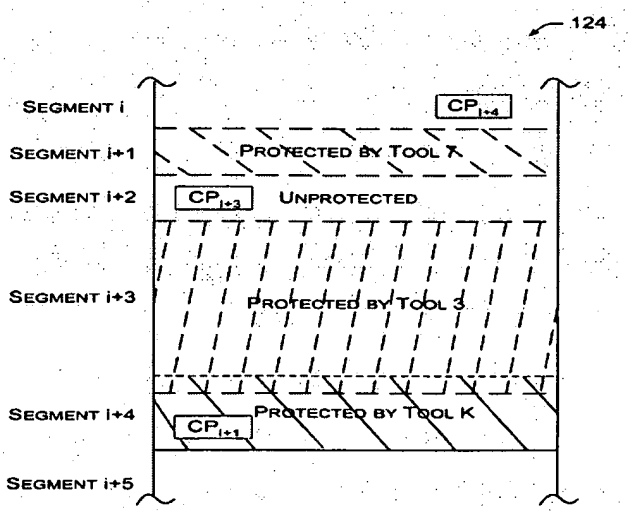


Fig. 4

f. Applicant's argued that none of the cited reference discloses *creating a simulation model using said obfuscated version of said electronic design.*

In response, applicants admitted:

> Applicant does agree that paragraph 72 indicates that the model compiler vendor (*i.e.*, the model compiler itself) is able to obfuscate the object code. Paragraphs 66 and 67 indicate that the model compiler accepts HDL source code and produces HDL object code in the form of linkable object files. It is clear that the obfuscation is performed by the model compiler after it inputs the HDL source code. But, claim 1 requires "creating a simulation model using said obfuscated version of said electronic design." Thus, the claim requires that the source electronic design is obfuscated before it is used to create a simulation model. By contrast, paragraph 72 of *Meyer* indicates that it is the model compiler itself that obfuscates the object code; the original HDL source code (without any obfuscation added to it) is input to the model compiler.

As applicant's admitted, the specification recited as follows:

> Next, a decision block 914 determines whether any other locations within the electronic design are available for obfuscation. If it is determined that other such locations are available for obfuscation, then process control returns to block 906 and operations 906, 908, 910, and 914 are performed as described above. These cycles of obfuscation continue until all pertinent locations within the IP core are considered. When no other locations remain for consideration, the obfuscation system has completed its task of inserting obfuscation circuitry in the IP core. At that point, the obfuscated IP core may be used provided as a simulation model – assuming that no format conversion is required (e.g., to Verilog). As shown, the system outputs the obfuscated circuitry at 916.

In light of the specification, the simulation model is not realized until it is fully compiled. The obfuscation is done before compilation is **complete**. Therefore, there is no model before compiling. After completion of compiling, there is a model as taught in the reference .

g. Applicant's argued that Koushanfar et al fails to disclose *inserting obfuscation circuitry into the region and producing a simulation model said optimized IP core that includes said inserted obfuscation circuitry.*

In response, Koushanfar et al discloses:

Page 2-3:

> One method to enable design IP protection is based on the constraint manipulation. The basic idea is to impose additional author-specific constraints on the original IP specification during its creation and/or synthesis. The copyright detector checks whether a synthesized IP block satisfies the author-specific constraints. The strength of the proof of authorship is proportional to the likelihood that an arbitrary synthesis tool incidentally satisfies all the added constraints [15,5,23]. Similarly, to protect legal users of the IP, fingerprints are added to the IP as extra constraints [4]. Finally, copy detection techniques for VLSI CAD applications have been developed to find and prove improper use of the design IP [6,16]. These techniques are effective for authentication. However, since they make each design unique, it becomes ill-suited for mass production and cannot be applied for hardware metering. In addition, obfuscation can be used for IP protection [7].

In this section, we propose and analyze a number of ways for hardware metering. There are several alternatives for implementing the identification logic within the control path logic for hardware protection. Our focus is on control logic, because in modern design it

Disconnection approach: In this approach, an additional finite state machine (FSM) is designed to facilitate design identification.

Checking the ID of the design, requires an unused state of the other FSMs that are part of the design. Modern designs have a large number of FSM with numerous unused states/input combinations (don't cares). The added FSM is the same for all the designs in the mask level. In the postprocessing step, lasers burn some of the connections of this added FSM in each design and thus generates different states and functions of it. This added FSM is different in each design since we laser burn different connections in each design to achieve a slightly different control path. The algorithms to decide exactly where to burn the interconnect in each chip, can be derived from a computer simulation of the state machine to derive unique ID for each of them. This solution does not need any extra processing steps and is much faster and more robust than the previous approaches.

h. Applicant's argued that none of the references discloses a simulation model that not only contains obfuscation circuitry but is also **cycle accurate and bit accurate**.

In response, Meyer et al discloses:

[0007] The current electronic system design steps are:

[0008] 1. Determine system specifications

[0009] 2. Verify correct architectural function.

[0010] 3. Convert specifications into HDL definition

[0011] 4. Verify correct system logic and timing

[0015] Currently, the most commonly used HDL is called Verilog. Another HDL is called VHDL. A number of new HDLs are under development such as Superlog and SDL. Many simulators are available for simulating correct logic and timing function of Verilog HDL models. Steps 3 and 4,

8. Examiner finds applicant's argument unpersuasive and is therefore the rejection maintained.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 25-36, 39, 42, 48, 54, and 57 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 25 and 39 recite "computer readable medium". Applicants specification (page 12) noted as follows:

> Some embodiments of the present invention relate to computer readable media or computer program products that include program instructions and/or data (including data structures) for performing various computer-implemented operations. Examples of computer-readable media include, but are not limited to, magnetic media such as hard disks, floppy disks, and magnetic tape; optical media such as CD-ROM disks; magneto-optical media; semiconductor memory devices, and hardware devices that are specially configured to store and perform program instructions, such as read-only memory devices (ROM) and random access memory (RAM). The data and program instructions of this invention may also be embodied on a carrier wave or other transport medium (including electronic or optically conductive pathways).

According to the above portion of the specification, the "medium" covers "carrier wave", which is *not a Manufacture within the meaning of 101.* In such embodiment, the program is still unable to act as a computer component and have its functionality realized.

To overcome the rejection a clear *disavowal is needed*.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claim 38 is rejected under 35 U.S.C. 102(b) as being anticipated by F. Koushanfar, and G. Qu, "hardware Metering" 2001 ACM.

As per Claim 38:

Koushanfar discloses a method of producing a simulation model of an intellectual property core, wherein the simulation model produces a hardware simulation result but cannot be directly compiled to produce a practical hardware implementation of the IP core, the method comprising:

(a) receiving a non-obfuscated version of the IP core in a native HDL format or in a partially compiled HDL format (**See: page 2, left side column, 22-25**);

(b) identifying a region of the non-obfuscated IP core where one or more flip-flops are located (**See: page 3, left side column, lines 4-12**);

(c) inserting obfuscation circuitry into the region (**See: page 2, left side column, lines 22-36**);

(d) adding additional flip-flops and/or modifying the flip-flops (**See: page 3, left side column, lines 2-5**); and

(e) optimizing the IP core after (c) and (d) have been performed (such as... ***GC optimization...***; **See: "6. Design Flow"**); and

(f) producing a simulation model using said optimized IP core that includes said inserted obfuscation circuitry (**See: page 4 "Conclusion"**).

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claim 39 is rejected under 35 U.S.C. 102(e) as being anticipated by Publication No. US 2002/0138244 A1 issued to Meyer et al.

As per Claim 39:

Meyer discloses a computer program product comprising a tangible computer readable medium on which is provided program instructions for implementing an intellectual property (IP) core said program instructions comprising:

a programming version of the IP core for insertion in an electronic design developed using a specified electronic design automation (EDA) platform (**See:** [0073]); and

a simulation model of the IP core for simulating operation of the IP core in the electronic design, wherein the simulation model includes comprises obfuscation

circuitry, absent in the programming version, which allows an accurate a hardware simulation result of the IP core but prevents direct compilation of the simulation model to produce a practical hardware implementation of the IP core **(See:[0072])**, said obfuscation circuitry increasing the area of said IP core or reducing the speed of critical path of said IP core (**See: [0072]**), said simulation model being cycle accurate and bit accurate (**See: [0007], [0009], [0011], [0015], [0033]**).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 1-5, 7, 8, 11-20, 23-32, 35, 36, 40-42, 44-48, and 50-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,080,257 issued to Jakubowski et al in view of Publication No. US 2002/0138244 A1 issued to Meyer et al.

As per Claim 1:

Jakubowski discloses a method of producing model of an electronic design, the method comprising:

receiving a non-obfuscated version of the electronic design suitable for direct compilation into a practical hardware implementation of the electronic design (**See: Fig. 2 #122 and corresponding texts; Col. 4 line 5-7**);

identifying a region of said electronic design into which a type of obfuscation may be added (**See: Fig. 2 #202 and corresponding texts);**

adding obfuscation circuitry to said electronic design to produce an obfuscated version of the electronic design, wherein said obfuscation circuitry prevents practical implementation of the electronic design on a target hardware device (**See: Col. 5 lines 55-64**);

creating model using said obfuscated version of said electronic design said simulation model being suitable for producing accurate hardware simulation results in a simulator but not being suitable to be directly compiled to produce a practical hardware implementation of the electronic design (**See: Fig. 2 # 124 and corresponding texts**); and

storing said simulation model in a computer system (**See: Fig. 1 # 108 and corresponding texts**).

Jakubowski teaches producing of protected digital goods such as software modules. However, Jakubowski is silent whether the protected digital goods are a simulation model results in a simulator.

Meyer discloses a simulation model results in a simulator (such as...***HDL simulator...***; **See: Abstract**).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Meyer et al with Jakubowski et al because both references are clearly concerned with protection of an intellectual property. The motivation for doing so would have been convenient to connect an HDL simulator, as taught by Meyer et al, to verify an electronic design.

As per Claim 2:

Meyer discloses a method as recited in claim 1, wherein the non-obfuscated version of the electronic design is provided in an HDL source format and said creating a simulation model includes using said obfuscated version of said electronic design as said simulation mode (**See: Abstract, [0072], [0101]**).

As per Claim 3:

Meyer discloses a method as recited in claim 1, wherein the electronic design is a reusable functional logic block (**See: [0026]**).

As per Claim 4:

Jakubowski discloses a method as recited in claim 1, wherein adding Obfuscation circuitry includes comprise: identifying a region for introduction of obfuscation circuitry in the non-obfuscated version of the electronic design; choosing a type of obfuscation circuitry for insertion; and inserting the chosen type of obfuscation circuitry into the identified region, thereby creating an obfuscated region (**See: Fig. 2 #**

202 and corresponding texts, Fig. 2 # 206 and corresponding texts, Fig. 4 and corresponding texts).

As per Claim 5:

Jakubowski discloses a method as recited in claim 4, wherein identifying a region for introduction of obfuscation circuitry includes comprises identifying in the non-obfuscated version of the electronic design logic of a type that is not removed by a synthesizer (**See: Fig. 2 # 202 and corresponding texts**).

As per Claim 7:

Meyer discloses a method as recited in claim 1, further comprising: optimizing the obfuscated version of the electronic design by merging the obfuscation circuitry with non-obfuscated functional circuitry of said obfuscated version (such as...***the preferred embodiment has the advantage that optimization and shrouding or obfuscation operation...***; **See: [0101]**).

As per Claim 8:

Jakubowski discloses a method as recited in claim 1, wherein the obfuscation circuitry increases the size of the electronic design without changing its function and/or slows the speed of the electronic design without changing its function (**See: Col. 6 lines 49-50**).

As per Claim 11:

Jakubowski discloses a method as recited in claim 1, wherein the obfuscation circuitry includes an comprises-a XOR tree (**See: Col. 9 lines 16-23**).

As per Claim 12:

Jakubowski discloses a method as recited in claim 1., wherein adding obfuscation circuitry is performed automatically without user intervention (**See: Col. 3 lines 31-33**).

As per Claim 13:

Jakubowski discloses an apparatus for producing a model of an electronic design, the apparatus comprising:

one or more processors (**See: Fig. 1 # 102 and corresponding texts**);

memory (**See: Fig 1 # 120 and corresponding texts**);

a design entry tool that allows a developer to input a non-obfuscated version of said electronic design (**See: Fig. 1 # 100**);

an obfuscation module for identifying a region of said electronic design (**See: fig. 2 #202 and corresponding text**) and adding obfuscation circuitry to said a non-obfuscated version of the electronic design to produce an obfuscated version of the electronic design from which the model can be created, wherein said obfuscation circuitry prevents practical implementation of the electronic design on a target hardware device (**See: Fig. 2 # 122 and corresponding texts; Col. 4 line 5-7**), said obfuscation module creating said simulation model, said model being suitable for producing accurate hardware results but not being suitable to be directly compiled to produce a practical hardware implementation of the electronic design (**See: Fig. 2 # 124 and corresponding texts**).

Jakubowski teaches producing of protected digital goods such as software modules. However, Jakubowski is silent whether the protected digital goods are a simulation model results in a simulator.

Meyer discloses a simulation model results in a simulator (such as ...***HDL Simulator...***; **See: Abstract**).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Meyer et al with Jakubowski et al because both references are clearly concerned with protection of an intellectual property. The motivation for doing so would have been convenient to connect an HDL simulator, as taught by Meyer et al, to verify an electronic design.

As per Claim 40:

Jakubowski discloses a method as recited in claim 8, wherein the obfuscation circuitry increases the area of the electronic design or reduces the speed of a critical path of the electronic design (**See: Col. 6 lines 49-50**).

As per Claim 46:

Meyer discloses a method as recited in claim 1 wherein said simulation model is cycle accurate and bit accurate (**See: [0033]**).

As per Claim 50:

Meyer discloses a method as recited in claim 38 further comprising: producing a simulation model using said optimized intellectual property core, wherein said simulation model is cycle accurate and bit accurate (**See: [0033]**).

As per Claim 52:

Meyer discloses a method as recited in claim 3 wherein said functional logic block is an intellectual property core (**See: [0078]**).

As per Claim 55:

Meyer discloses a method as recited in claim 1, wherein the non-obfuscated version of the electronic design is provided in a partially compiled format, and wherein said creating a simulation model includes using a translation utility to convert said obfuscated version of said electronic design into said simulation model having a standard format usable by a variety of simulators (**See: [0073]**).

17. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patent No. 7,080,257 issued to Jakubowski et al in view of Publication No. US 2002/0138244 A1 issued to Meyer et al as applied to claims 1-5, 7, 8, 11-20, 23-32, 35, 36, 40-42, 44-48, and 50-57 above, and further in view of F. Koushanfar, and G. Qu, "hardware Metering" 2001 ACM.

As per Claim 6:

Jakubowski fails to disclose one or more flip-flops.

Koushanfar discloses a method as recited in claim 5, wherein the type of logic that is not removed by a synthesizer includes comprises one or more flip-flops (such as ...***Finite State Machine...***; **See: page 3, left side column, lines 4-5**).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Koushanfar et al with Jakubowski et al because both references are clearly concerned with protection of an intellectual property. The motivation for doing so would have been convenient to connect additional

Finite State Machine which comprises a flip-flops, as taught by Koushanfar et al, to achieve a slightly different control path.

As per Claims 14-20, 23-32, 35, 36, 41-44, 47, 48, 50, 53, 54, 56, and 57:

The limitations of claims 14-20, 23-32, 35, 36, 41-44, 47, 48, 50, 53, 54, 56, and 57 have already been discussed in the rejection of claims 1-8, 11, 12, 40, 46, 52, and 55. The instant claims are functionally equivalent to the above rejected claims and are therefore rejected under the same rationale.

Allowable Subject Matter

18. Claims 37, and 49 are allowed.

19. The following is an examiner's statement of reasons for allowance:

The prior art of reference expressly fails to disclose the limitation of:

As claim 37, ***inserting entangler circuitry upstream from the region and inserting complementary detangler circuitry downstream from the region***; and

inserting scrambler circuitry upstream from the region and inserting complementary descrambler circuitry downstream from the region.

As claim 49, it depends on claim 37 and therefore allowed.

20. Claims 9, 10, 21, 22, 33, and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of reference expressly fails to disclose the limitation of:

As per claim 9, ***adding circuitry for scrambling an input signal by spreading out the input signal in time***; and ***adding circuitry for de-scrambling an output signal resulting from the circuitry for scrambling***,

As per claim 10, ***adding circuitry for entangling multiple input signals to thereby spread out the input signals; and adding circuitry for detangling an output signal resulting from the circuitry for entangling.***

As per claims 21, 22, 33, and 34, the same statement of reasons for allowance will apply as claim 9, and/or 10 because they have similar limitation as of claims 9 and/or 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

22. Claims 1-8, 11-20, 23-32, 35, 36, 38-42, 44-48, and 50-57 are rejected.

23. Claims 37, and 49 are allowed.

24. Claims 9, 10, 21, 22, 33, and 34 are objected.

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is 571-272-8571. The examiner can normally be reached on 8:00 am - 4:30 pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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